Technical Note

I^{2}C Communication with Honeywell Digital Airflow Sensors

1.0   Introduction

The I^{2}C bus is a simple, serial 8-bit oriented computer bus for efficient I^{2}C (Inter-IC) control. It provides good support for communication between different ICs across short circuit-board distances, such as interfacing microcontrollers with various low speed peripheral devices. For detailed specifications of the I^{2}C protocol, see **I^{2}C Bus Specification Version 2.1 January 2000.** Source: NXP Semiconductor at http://www.nxp.com/acrobat_download/literature/9398/393400 11.pdf. (Note: this link is controlled by NXP Semiconductor and is subject to change by them.)

Each device connected to the bus is software addressable by a unique address and a simple master/slave relationship that exists at all times. The output stages of devices connected to the bus are designed around an open collector architecture. Because of this, pull-up resistors to +V$_{DD}$ must be provided on the bus.

Both SCL and SDA are bidirectional lines, and it is important to system performance to match the capacitive loads on both lines. In addition, in accordance with the I^{2}C specification, the maximum allowable capacitance on either line is 400 pF to ensure reliable edge transitions at 400 kHz clock speeds (see Figure 1). When the bus is free, both lines are pulled up to +V$_{DD}$. Data on the I^{2}C-bus can be transferred at a rate up to 100 kbit/s in the standard-mode, or up to 400 kbit/s in the fast-mode.

Figure 1. I^{2}C Bus Configuration
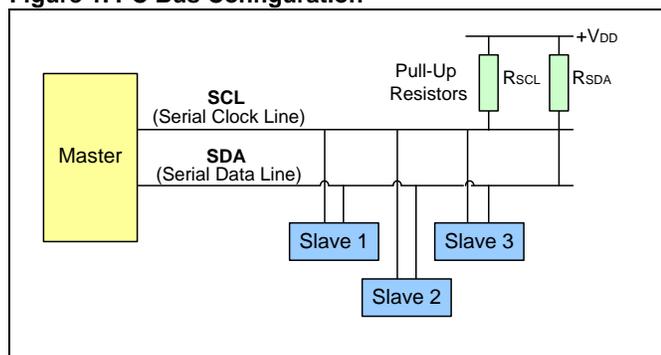
2.0   Sensor Address

Each I^{2}C digital sensor is referenced on the bus by a 7-bit slave address. The I^{2}C default address is 0x49; however, the address is selectable according to the Nomenclature and Order Guide in the Honeywell Zephyr™ Digital Airflow Sensors: HAF Series-High Accuracy product data sheet.

(Other custom values are available. Please contact Honeywell Customer Service if there are questions regarding custom slave addresses.)

3.0   Digital Flow Reading

Honeywell's digital output airflow sensors are designed to work as slaves and will therefore only respond to requests from a master device. The sensors operate as a slave-only and the READ command structure is shown in Figure 2.

The sensors report the "data not ready" status until after a start-up time. The first two consecutive READ commands that respond with non-zero valid data will provide the contents of two 16-bit registers with serial number information.

Figure 2. Standard I^{2}C READ Command and Word Structure
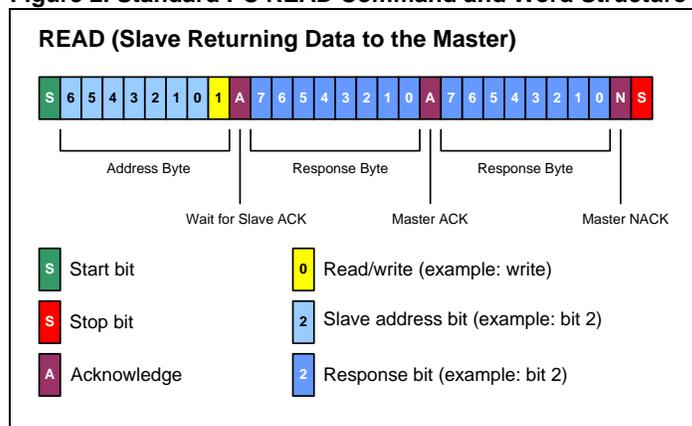
The sensor is asynchronous at start-up and will wait to supply the sequential serial number values on the first two READ commands.

After the serial number registers are read in succession, the sensor will then begin repeating 14-bit calibrated flow sensor output values updated every 1 ms (I^{2}C 16-bit word including two leading zero bits = '00' specifying calibrated flow data packet). Table 1 shows the initial start-up sequence and subsequent data transfers of the sensor after power is applied.

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Table 1. Start-up Sequence

Data	I²C Transfer 1	I²C Transfer 2	I²C Transfer 3	I²C Transfer 4
Received by airflow sensor	slave address with read bit	slave address with read bit	slave address with read bit	slave address with read bit
Command	I²C read op	I²C read op	I²C read op	I²C read op
Transmitted by airflow sensor	0x0000	Data [15:0]	Data[15:0]	{00, Data[13:0]}
Response	diagnostic low	customer Reg0	customer Reg1	corrected flow
Comment	data not ready	data ready, send serial number register 0 once	send serial number register 1 once	start sending flow for successive reads

Note: The leading 2-bits of each word of the 14-bit sensor output data are '00'.

4.0 Parameter Specifications and Timing

Table 2 describes the minimum and maximum limits for parameters for I²C operation with the Honeywell airflow sensors.

Table 2. Parameters for I²C Bus Communication with Honeywell Digital Airflow Sensors

Characteristic	Sym.	Condition	Min.	Typ.	Max.	Unit	Note
Input high level	V_{IH}	–	0.9	–	1	V_{DD}	1
Input low level	V_{IL}	–	0	–	0.1	V_{DD}	1
Output low level	V_{OL}	open drain, I_{OL} = -4 mA	–	–	0.1	V_{DD}	1
Pull up current	I_{OH}	pins SCL and SDA	5	–	20	µA	–
Load capacitance SDA	C_{L_SDA}	–	–	–	400	pF	–
SCL clock frequency	f_{SCL}	–	–	–	100	kHz	–
Bus free time between STOP and START condition	t_{BUF}	–	4.7	–	–	µs	–
Hold time (repeated) START condition	$t_{HD,STA}$	to first clock pulse	4.0	–	–	µs	–
Low period of SCL	t_{LOW}	–	4.7	–	–	µs	–
High period of SCL	t_{HIGH}	–	4.0	–	–	µs	–
Setup time repeated start condition	$t_{SU,STA}$	–	4.7	–	–	µs	–
Data hold time	$t_{HD,DAT}$	–	0	–	–	ns	–
Data setup time	$t_{SU,DAT}$	–	250	–	–	ns	–
Rise time of both SDA and SCL	t_R	–	–	–	300	ns	–
Fall time of both SDA and SCL	t_F	–	–	–	300	ns	–
Set up time for stop condition	$t_{SU,STO}$	–	4	–	–	µs	–
Input filter spike suppression	t_{SP}	spikes on SDA or SCL of that length are suppressed	–	–	50	ns	–

Note:

1. V_{DD} is the supply voltage.

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⚠ WARNING

PERSONAL INJURY

DO NOT USE these products as safety or emergency stop devices or in any other application where failure of the product could result in personal injury.

Failure to comply with these instructions could result in death or serious injury.

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